A CHARGE MODEL OF STEP RECOVERY DIODE FOR CAD

Katarzyna Opalska and Jerzy Baranowski

Institute of Electronics Fundamentals
Warsaw University of Technology
Warsaw, Poland

ABSTRACT

A physics-based, numerically efficient model of Step Recovery Diode (SRD) is presented. The model, based on partitioning of charge in the diode base into sections, has been implemented in generic circuit simulators and tested in simulations of variety of pulse circuits. It has been also verified by comparison of measurement data and model analysis results. The verification confirmed the model ability to represent accurately SRD pulse behaviour for a wide range of diode operating conditions.

INTRODUCTION

Step recovery diodes remain extremely useful in a variety of pulse circuits, like wave-shaping circuits and frequency multipliers, since their introduction in sixties [1]. However, there still does not exist a standard SRD model suitable for CAD, that would be both accurate and numerically efficient. The models reported in literature usually describe the device only behaviorally, e.g. they render pertinent to SRD long delay time and fast slopes by two switched capacitances of different values (assuring charge continuity in such a model was described only recently in [4]). Unfortunately such a model is too simplistic to correctly render neither the details of SRD switching (especially during fast turning off) nor the diode behaviour for varying excitations in the circuits.

In this paper a lumped, physics-based, yet accurate and numericaly efficient SRD model is presented. The model is based on the charge-section method introduced in [2]. The original SRD model presented in [2] consisted of nonlinear capacitances and nonlinear controlled sources. The model presented in this paper has been derived directly from the charge-section description of the diode. As a consequence the new model uses section charges as independent variables rather than voltages across nonlinear capacitors. Thus, only linear capacitances and nonlinear control sources are used. The charge-oriented model description, along with some numerical tricks (like scaling the physical values of parameters to the values meaningful to the circuit simulator) improves both efficiency and accuracy of computer simulations. The presented model has been implemented in several generic circuit simulators (the `SPICE-3` implementation is included in the paper). The model has been also verified by comparison of measurement data and model analysis results. The verification confirmed the model ability to represent accurately SRD pulse behaviour for a wide range of diode operating conditions, which is illustrated in the paper. An example of the analysis of a pulse circuit closes the presentation.

PARTITIONED CHARGE - BASED SRD MODEL

The principles of the charge section method

The charge section method relies on:

1. one-dimensional partitioning of diode base into parts and treating the charge in each part as resulting from superposition of 2 "charge sections" responsible for forward and reverse carrier transmission;
2. modeling separately charge of each section (in a basic approach by a linear differential equation);
3. determining the boundary conditions for each section.

SRD model construction

Fig. 1 examplifies partitioning of the total charge of (one polarity) carriers in SRD base into 4 sections. Q^1, Q^3 sec-

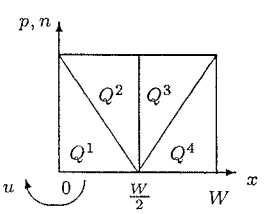

Fig. 1. Partitioning SRD base charge into 4 sections.

tions represent forward and Q^2, Q^4 - reverse carrier transmission. Current flow through charge sections is shown in Fig. 2.The input and output currents of each section are defined as:

$$i^i_{in} = \frac{d(Q^i - Q^i_0)}{dt} + \frac{Q^i - Q^i_0}{\tau} + i^i_{out} \quad (1)$$

$$i^i_{out} = \frac{Q^i - Q^i_o}{t_t} \quad (2)$$

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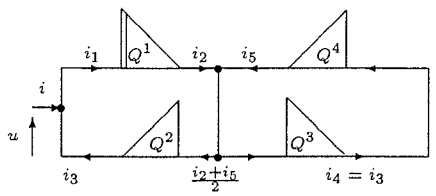

Fig. 2. Current flow through charge sections in diodes base assuming ideal contact at the base end ($l-h$ junction.)

where Q_0^i is a thermodynamically balanced charge and τ, t_t - are the carrier lifetime and the transit time respectively. Due to physical phenomena occuring inside SRD structure both carrier lifetime and transit time depend on diode voltage (yet the model is still considered quasi-static). The transit time t_t depends on the effective base width W_{eff}, which in turn depends on the diode voltage U_D. Finally, t_t decreases with diode voltage up to the punch through (for $U_D = U_p$), when $W_{eff} \to 0$ and transit time equals to the small convection time t_{ts0} only. The transit time for the whole range of diode voltages is defined as:

$$t_t = t_{t0}\Big[1 - \sqrt{\frac{\Phi_d - max(U_D, -U_p)}{\Phi_d + U_p}}\Big]^2 + t_{ts0} \qquad (3)$$

The carrier lifetime τ is assumed constant in the basic model. In a more complex version of the model τ can be a variable depending on dynamically changing level of total base charge, e.g. according to the heuristic formula:

$$\tau = \tau_0 \frac{1 + aQ_{tot}}{1 + bQ_{tot}} \quad , \quad Q_{tot} = \sum_i Q_i \qquad (4)$$

The charge of the first section (next to the $p-n$ junction), depends on the voltage U_D applied to a diode. For the typically assumed exponential recombination model, this charge equals to:

$$Q^1 = Q_0^1 exp\frac{U_D}{nU_T} \qquad (5)$$

The excess charge $Q^1 - Q_0^i$ equals then:

$$Q^1 - Q_0^1 = Q_0^1(exp\frac{U_D}{nU_T} - 1) \qquad (6)$$

The charges of other sections depend only on their boundary conditions (assuming ideal contact at the base end). Those charges obviously depend on junction voltage, but indirectly - via charges and currents of neighboring sections.

Circuit diagram of SRD model

Fig. 3 shows a circuit representation of formulas (1,2) for a single charge section. The circuit from Fig. 3 may be modeled directly in a generic circuit simulator. If the simulator does not support elements described by charge equations (e.g. SPICE family), the Q variable can be represented as an

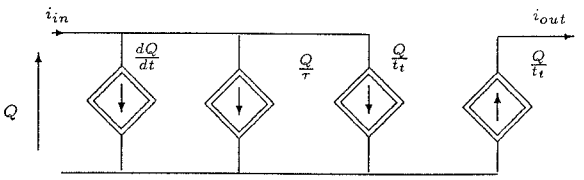

Fig. 3. Circuit representation of a single charge section.

equivalent voltage. As an example, Fig. 4 illustrates modeling of a nonlinear charge section in SPICE-like simulators. The non-inertial diode D has exponential characteristic like the one described by (6). The linear capacitor C_Q differentiates nonlinear charge Q, while R_Q is just the scaling resistor needed to change diode current into equivalent voltage.

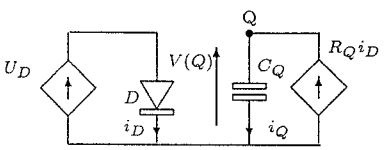

Fig. 4. SPICE representation of a nonlinear charge model.

The core of the SRD model (the intrinsic model) consists of subcircuits shown in Fig. 3 connected according to Fig. 2. Let us note here, that the resulting model consist only of 3 sections, because sections 2 and 3 may be combined together, as they are controlled by the same voltage.

The full SRD model is additionally enhanced by the following components (see Fig. 5):

- serial resistance R_S (assumed constant here),
- junction capacitance C_J (dependent on U_D through W_{eff}),
- noninertial diode D_N representing non-ideal current due to carrier surface recombination,
- package parasitic parameters L_0, C_0.

In what follows we assume, that the first 3 components from the above list also belong to the SRD model, leaving aside the package parameters (which may be easily included in circuit simulation as external elements). There are 11 pa-

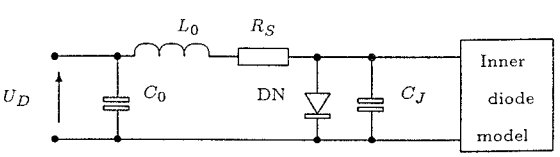

Fig. 5. Full circuit diagram of the SRD model.

rameters in such a model formulation: thermodynamically balanced charge Q_0, non-ideality coefficient n, constant carrier lifetime τ_0, normalized transit time t_{t0}, convection time t_{ts0}, zero-bias junction capacitance C_{j0}, diffusion potential

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Φ_d, punch-through voltage U_p, serial resistance R_S, saturation current of non-ideal diode I_{Sn} and its non-ideality coefficient n_n. The model with variable carrier lifetime (according to eq. (4)) has 2 additional parameters: a, b.

SRD model implementation

Fig. 6 presents a parametrized description of the SRD model as a subcircuit in SPICE-3f simulator.

```
* CHARGE-BASED SRD MODEL
.SUBCKT SRD hi lo
*     Serial resistance
RSER hi sec1 {Rs}
*     Nonideal diode
DN sec1 lo DNONID
.MODEL DNONID D (IS={Isn} N={Nn})
*     Junction capacitance
XCJ sec1 lo  CJ
.SUBCKT CJ 1 2
Bx QJ 0 V=-2*{Cj0}*{Fid}*sqrt(1- max( min(v(1,2),{.95*Fid}),
+ {-Up})/{Fid} )+ {Cj0}*min(v(1,2)+{Up},0)/sqrt(1+{Up}/{Fid})
Fx 2 1 Bx 1
.ENDS CJ
*Charge of the first (nonlinear) section
EQ1 int1 0 sec1 lo 1
DQ int1 0 DID
.MODEL DID D (IS={Q0} N={n})
HQ2 intQ 0 EQ1 -1
CQ intQ 0 1n
* Dynamic model parameter
BTT TT 0 V={tt0*1e9}*( 1- sqrt (min(max({Fid}-V(sec1,lo),0),
+ {Fid+Up})/({Fid+Up}))^2+{tts0*1e9}
BCHARGE CHARGE 0 V=V(sec4,lo) + V(sec2,lo)*2+V(intq)
* Switch constant/variable tau
* - choose one of the following lines
*BTAU TAU 0 V={tau0*1e9} * (1+{a*b}*V(charge))/(1+{a}*V(charge))
Vtau TAU 0 {tau0*1e9}
* The first, nonlinear charge section
B11 sec1 lo I=(V(intq)-V(sec2,lo))/V(tt)+ V(intq)/V(tau)-I(HQ2)
* The second and third charge sections combined
C2 sec2 lo 2n
B21 lo sec2 I=(V(intq)+V(sec4,lo)+1e-12)/V(tt)
B22 sec2 lo V=(I(B22)+1e-12)/2/(1/V(tau) + 1/V(tt))
* The fourth charge section
C4 sec4 lo 1n
B41 lo sec4 I=(V(sec2,lo))/V(tt)
B42 sec4 lo V=I(B42)/(1/V(tau) + 1/V(tt))
.ENDS SRD
```

Fig. 6. SRD model as a subcircuit in a SPICE-3 simulator.

MODEL VERIFICATION

The presented SRD model was experimentally verified by comparison of the model responses against the following measurement data:

- static characteristic $I_D(U_D)$;
- switching time waveforms for different excitations (I_F, I_R), as measured in the circuit shown in Fig. 8.

Model parameters were extracted using standard optimization routines. Results obtained for tens of devices confirmed very good model fit for all available measurement data. Fig. 7 shows excellent agreement of measured and modeled static diode characteristic and Figs. 9, 10 demonstrate fit for time responses as measured in circuit from Fig. 8.

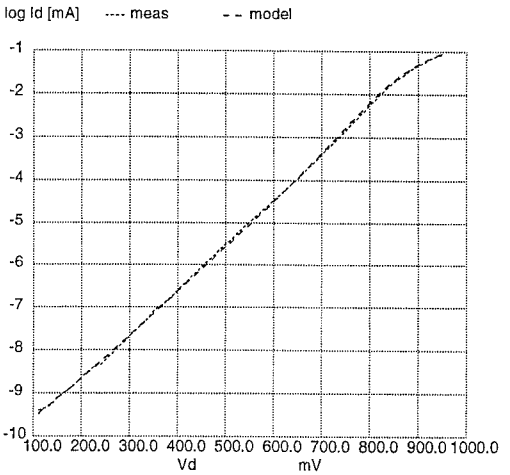

Fig. 7. Model fit of static SRD characteristic.

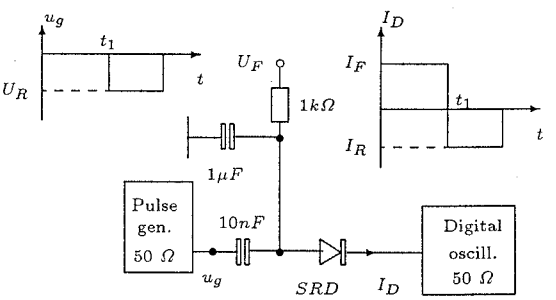

Fig. 8. Test circuit for measurements of current time waveform during switching

Model validity was confirmed in a broad range of diode operating conditions, including those not taken into account during model parameter extraction (an example of such a point is shown in Fig. 10). For comparison, Figs. 9, 10 include also simulation results for the same circuit with the model presented in [4][1]. For this model we were able to find parameter set from a single waveform (Fig. 9). However, varying excitation in the measurement circuit made the model fit quite unsatisfactory (see Fig. 10), while the proposed model remained accurate.

EXAMPLE OF CIRCUIT ANALYSIS

The presented model has been implemented in several generic circuits analysers (e.g. NAP-2, SPICE-3, PSPICE-5) and tested in simulation of different pulse circuits with excellent results. Fig. 11 presents a sample circuit for shaping a narrow pulse from almost arbitrary input and Figs. 12, 13 - the results of its computer simulation.

[1]The model has been implemented by the authors in SPICE-3 simulator for testing purposes.

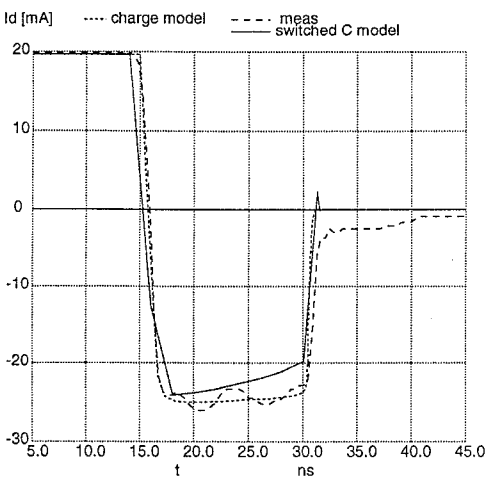

Fig. 9. Diode current response measured in circuit from Fig. 8 (dotted line denotes the charge model, solid line - the model as in [4], dashed line - measurements); $I_F \approx 20mA, B = \frac{I_R}{I_F} \approx 0.6$

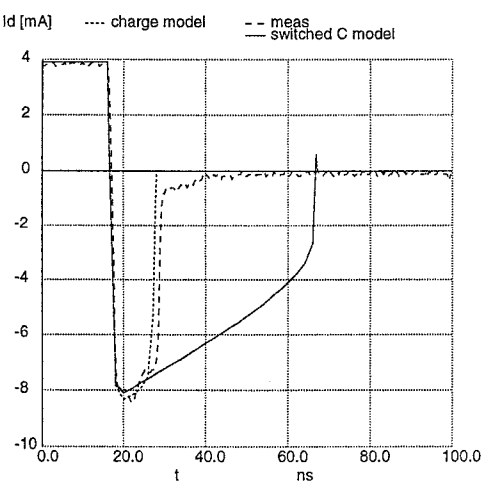

Fig. 10. Diode current response measured in circuit from Fig. 8; conditions not used in model characterization ($I_F \approx 4mA, B \approx 2.2$).

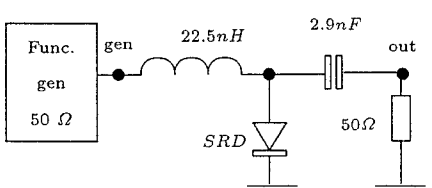

Fig. 11. A test circuit with SRD shaping a narrow pulse from sinusoidal or exponential input waveform.

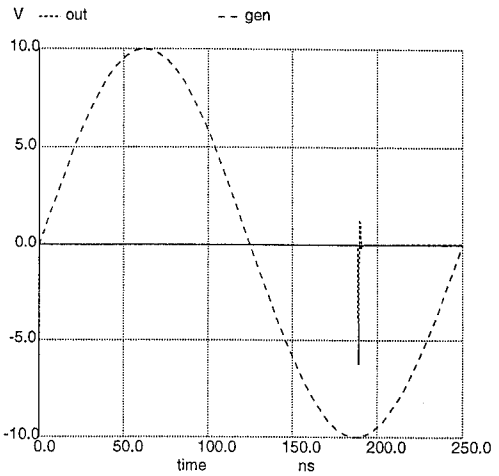

Fig. 12. Simulation results for the circuit from Fig. 11: output voltage together with input one.

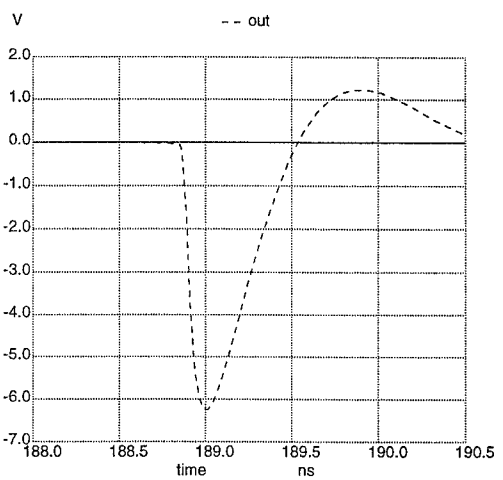

Fig. 13. Simulation results for the circuit from Fig. 11: zoomed in output pulse (300 ps width).

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